

option

report, Scope 1200B 405 TV conversion.pdf.

1 Why

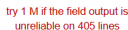
parts.

one.

2 The circuit (figure S3)

Figure S3: alternative sync separator using the LM1881 (replaces fig 01)

Same outputs as fig 01: LINE SYNC positive pulses 0 → 12 V (also line blanking), FIELD SYNC active low. Untested starting values: keep fig 01 as the fallback.



- RSET sets the chip's internal timing for the line rate: 680 k is the 625/525 value, 405 lines run 35 % slower, so ~ 1 M may suit them better.

Pin	Function	Connection
2	Composite video in	VIDEO IN through C1, 0.1 μ F. It takes 0.5–2 V p-p with sync going negative, which is standard 1 V video
6	RSET	680 k to 0 V with 0.1 μ F across it. Try 1 M on 405 lines (§4)
8	VCC	+12 V, with 100 nF and 10 μ F at the pin
4	Ground	0 V

1	Composite sync out, low on sync	4.7 k pull-up to +12 V, then through Q1 to LINE SYNC
3	Vertical sync out, low on field sync	4.7 k pull-up to +12 V; it's FIELD SYNC
5, 7	Burst gate, odd/even field	Not used

It gives the same outputs as fig 01, so figs 02, 03 rev B, 05 and 06 don't change:

- **LINE SYNC: positive pulses, 0 → 12 V.** Q1 (BC548) inverts the LM1881's low-going composite sync, as fig 01's Q3 did. These pulses empty fig 02's timing capacitor and act as line blanking in the video amplifier. The 10 k from Q1's base to emitter keeps Q1 firmly off when pin 1 is low, which can be up to about 0.8 V.
- **FIELD SYNC: active low.** It goes straight to fig 03 rev B's 4.7 k input.
 - **Why the pull-up matters:** fig 03's discharge transistor is a BC557 whose emitter rises to about 7.6 V. FIELD SYNC must rise nearly to 12 V to switch it off cleanly. The 4.7 k pull-up makes sure it does, whatever the chip's own output stage does.
 - **Field blanking:** fig 03 rev B's Q4 makes FIELD BLANK from the same signal, as before.

Supply: the LM1881 runs on 5–12 V, with an absolute maximum of 13.2 V. The IRM-10-12's 12 V is fine. Keep the 75 Ω termination at VIDEO IN: one termination for the whole box, which also feeds the video amplifier.

3 Parts

Part	Qty	Note
LM1881N (DIP-8) and an 8-pin socket	1	Your stock
BC548 (or BC547/BC549)	1	Your stock
680 k, plus 1 M to try	1 + 1	RSET
4.7 k	2	Pull-ups on pins 1 and 3
10 k	2	Q1 base resistor and base-to-emitter resistor
4.7 k	1	Q1 collector load
0.1 μF	3	C1, RSET decoupling, pin 8 decoupling
10 μF 16 V	1	Pin 8 decoupling
75 Ω	1	Input termination, if not already on the video amplifier board

The fig 01 parts on the add-on box parts list (S-Q1–Q4 and S-R, S-C) aren't needed if this version works.

4 On 405 lines

The LM1881 is specified for 525- and 625-line video (and similar rates), but the parts that matter here don't depend on the line rate:

- **Composite sync (pin 1):** a slicer that follows the sync pulses at any rate. 10,125 Hz is fine.
- **Field sync (pin 3):** the chip signals a field when sync stays low much longer than a line pulse. 405-line field sync is made of long broad pulses, so it easily qualifies.
- **RSET:** sets the chip's internal timing. It's scaled for the line rate, and 680 k is the value for 625 and 525 lines. 405 lines run about 35 % slower, so if the field output is missing or erratic on 405 lines, try **1 M**. The burst-gate and odd/even outputs also depend on this timing, but they aren't used.

If the field output is still unreliable on 405 lines with 1 M, go back to fig 01. Its field integrator was designed for both standards.

5 Testing

Apply 405-line video from the test-pattern generator or the standards converter, and look with the PicoScope:

1. **Pin 1:** clean composite sync, low on each sync pulse, about 9 μ s line pulses at 10,125 Hz, and the broad pulses at the start of each field.
2. **Pin 3:** one low pulse per field, 50 per second.
3. **Q1 collector (LINE SYNC):** positive pulses swinging about 0 $\rightarrow$ 12 V.
4. **FIELD SYNC at fig 03's input:** high at about 12 V between pulses, so fig 03's discharge transistor is fully off during the scan.
5. **Repeat on 625 lines** (15,625 Hz) if you'll use that too.
6. **Then the picture:** with fig 02 and fig 03 running, the raster should lock immediately and hold steady when you change channel or source.

6 Results

Check	Result
RSET value used	680 k (first test)
405 lines: line lock, field lock	3 Oct 2026, Domino source: line period about 98 μ s (10,125 Hz), field pulses every 20 ms with RSET 680 k. 1 M not needed. Lock with the timebases still to check
625 lines: line lock, field lock	3 Oct 2026: line pulses at about 15.6 kHz on pin 1. Field sync on pin 3 low-going (correct) and behaving as expected. Q1 collector (LINE SYNC): positive pulses, correct. Lock with the timebases still to check
Kept, or went back to fig 01	LM1881 works on both standards; kept (subject to the timebase lock check)